REMARKS

Claims 1-10 and 12-23 were examined and reported in the Office Action. Claims 1-10 and 12-23 are rejected. Claims 2 and 21 are canceled. Claims 1-10 and 18 are amended. Claims 1, 3-10, 12-20 and 22-23 remain.

Applicant requests reconsideration of the application in view of the following remarks.

35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-20 are rejected in the Office Action under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 6,181,151 issued to Wasson ("Wasson"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)) Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of " [a] apparatus comprising: an integrated circuit, said integrated circuit including: a test controller having an instruction register and a test access port finite state machine (TAP FSM), said test controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal; at least one logic unit controller; a single

test bus directly coupled between the test controller and the at least one logic unit controller; at least one design-for-test-feature coupled to the at least one logic unit controller; and a logic unit coupled to the at least one design-for-test-feature wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said integrated circuit, said logic unit controller generates a local shift signal and a local load signal from the packet, wherein said integrated circuit performs tests and generates test signals directly on said integrated circuit."

Applicant's amended claim 10 contains the limitations of " platform comprising: a support structure; a controller disposed on the support structure and coupled to an input device; at least one memory chip disposed on the support structure and coupled to the controller through a processor bus, said controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal; and an integrated circuit having a test controller having an instruction register and a test access port finite state machine (TAP FSM), at least one logic unit controller, a single test bus directly coupled between the test controller and the at least one logic unit controller, at least one design-for-test-feature coupled to the logic unit controller, and a logic unit coupled to the at least one design-for-test-feature, said logic unit controller generates a local shift signal and a local load signal from the packet, wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said platform and said integrated circuit performs and generates test signals directly on said integrated circuit."

Applicant's amended claim 18 contains the limitations of " [a] method comprising: generating a test information packet in a test controller of an integrated circuit; transmitting the test information packet to at least one logic unit controller over a single test bus directly coupled between the test controller and the at least one logic unit controller; processing the test information packet within the at least one logic unit controller to generate a local shift signal and a local load signal; transmitting the local shift signal and the local load signal to the at least one design-for-test-feature coupled to the logic unit controller, wherein said local shift signal and said local load signal are generated on said integrated circuit to perform tests on said integrated circuit."

Applicant's claimed invention tests and debugs an integrated circuit where the integrated circuit contains all necessary components for carrying out the testing or debugging directly on the integrated circuit. That is, the integrated circuit to be tested generates its own test signals. The distributed test control scheme reduces the number of global test control lines. For example, a load signal and a shift signal are transmitted together in a packet over a single test bus in a global test signal, as compared to the prior art that transmitted load and shift signals over separate global test control lines, in separate global control signals. Therefore, Applicant's claimed invention relaxes routing constraints on the test control lines, and adds greater flexibility in the physical placement of the test controller and test control logic.

Wasson discloses an integrated circuit (IC) tester 10. It is asserted in the Office Action that the integrated circuit tester illustrated in Figure 1 is all on one single integrated circuit and that the tester is part of the DUT, based on Figure 1 showing the DUT as part of tester 10. The DUT, however, is replaceable with other DUTs to be tested. One of ordinary skill in the art would know that tester 10 can test different types of devices and the devices to be tested are then coupled to the specific channels necessary. That is why tester 10 can test different ICs and PLDs, as indicated by the description.

The test instructions in Wasson are stored on system disk drive 17 and transmitted to tester channels through memory bus 24 (See Wasson, column 4, lines 57-67). Wasson simply does not disclose, teach or suggest that a global control signal is comprised of a packet, where the packet contains shift and load signals. Nor does Wasson teach, disclose or suggest that a logic unit controller that receives the global signal generates two local signals, a local shift signal and a local load signal.

Therefore, Wasson does not teach, disclose or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above. Specifically, Wasson does not teach, disclose or suggest "said test controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal; at least one logic unit controller; a single test bus directly coupled between the test controller and the at least one logic unit controller; at least one design-for-test-

feature coupled to the at least one logic unit controller; and a logic unit coupled to the at least one design-for-test-feature wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said integrated circuit, said logic unit controller generates a local shift signal and a local load signal from the packet, wherein said integrated circuit performs tests and generates test signals directly on said integrated circuit," nor "processing the test information packet within the at least one logic unit controller to generate a local shift signal and a local load signal; transmitting the local shift signal and the local load signal to the at least one design-for-test-feature coupled to the logic unit controller, wherein said local shift signal and said local load signal are generated on said integrated circuit to perform tests on said integrated circuit."

Since Wasson does not disclose, teach or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 10 and 18 are not obvious over Wasson since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 1, 10 and 18, namely claims 2-9, 12-17, and 19-20, respectively, would also not be obvious over Wasson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejections for claims 1-20 is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1, 3-10, 12-20 and 22-23, patentably defines the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN

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By _____
Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on January 14, 2005.

Nedy Calderon

Nedy Calderon